

REMARKS

Claims 1-42 remain present in this application.

Claims 16-23 stand rejected under 35 USC 102(b) as being anticipated by Chen et al., U.S. Patent 6,239,011. This rejection is respectfully traversed.

Claims 35-42 stand rejected under 35 USC 102(b) as being anticipated by Chen et al. This rejection is respectfully traversed.

With regard to the rejection of claims 16-23, independent claim 16 has been amended to incorporate the limitations of claim 17, as follows (emphasis added):

16. A semiconductor structure with a partially etched gate, comprising:
 - a semiconductor substrate;
 - a gate dielectric layer, a gate conductive layer and a cap layer, sequentially stacked on the substrate to form a gate structure;
 - a lining layer disposed on sidewalls of the gate structure, wherein the lining layer disposed on one sidewall of the gate structure is partially etched to expose the adjacent gate structure;
 - an inter-layer dielectric layer covering the gate structure; and
 - a contact formed in the inter-layer dielectric layer, *exposing the substrate and a portion of the cap layer of the gate structure therein, wherein the lining layer of the exposed portion of the gate structure is partially removed.*

It is respectfully submitted that Chen et al. neither teaches nor suggests all of the limitations set forth in independent claim 16. Specially, it is respectfully submitted that Chen et al. fails to teach or suggest a contact formed in the inter-layer dielectric layer, exposing the substrate and a portion of the cap layer of the gate structure therein, wherein the lining layer of the exposed portion of the gate structure is partially removed. Accordingly, reconsideration and withdrawal of the 35 USC 102(b) rejection of independent claim 16 and its dependent claims are respectfully requested.

With regard to the rejection of independent claim 35 and its dependent claims, it is noted that independent claim 35 recites (emphasis added):

35. A semiconductor structure with a partially etched gate, comprising:
a semiconductor substrate;
a gate dielectric layer, a gate conductive layer and a cap layer, sequentially stacked on the substrate to form a gate structure; and
a lining layer disposed on sidewalls of the gate structure, wherein *the lining layer disposed on two sidewalls of the gate structure is partially etched to expose the adjacent gate structure.*

It is respectfully submitted that the specification and figures of Chen et al. fail to teach or suggest formation of an gate structure with a partially etched lining layer disposed on sidewalls thereof. Specially, it is respectfully submitted that Chen et al. fails to teach or suggest the lining layer being disposed on two sidewalls of the gate structure being partially etched to expose the adjacent gate structure. Accordingly, reconsideration and withdrawal of the 35 USC 102(b) rejection of independent claim 35 and its dependent claims are respectfully requested.

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

Application No. 10/695,739
Amendment dated September 6, 2005
Reply to Office Action of June 3, 2005

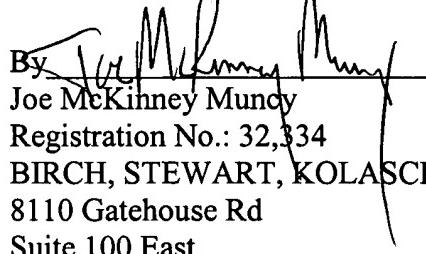
Docket No.: 0941-0860P

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: September 6, 2005

Respectfully submitted,

By


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